In the Claims:

Please cancel claims 2, 8, and 26, and amend claims 1, 3, 24, 27, and 28. The status of all claims is as follows:

1. (Currently Amended) A chip comprising:

an array of hexagonal cells;

a plurality of interconnects including a plurality of Y's, each of the Y's respectively connecting the cells in clusters of three cells each, wherein the cells within the clusters are interconnected;

wherein the Y connecting each cluster has a node and three interconnects, each of the three interconnects having an end that connects the node to a respective one of the cells within a cluster;

wherein each Y connects each cell of its respective cell group to the node.

2. (Cancelled)

3. (Currently Amended) A chip comprising:

an array of hexagonal cells;

a plurality of interconnects including a plurality of Y's, each of the Y's respectively connecting the cells in clusters of three cells each, wherein the cells within the clusters are interconnected;

wherein the Y connecting each cluster has a node and three interconnects connecting the node to respective ones of the cells within a cluster;

wherein each Y connects each cell of its respective cell group to the node;

~~The chip of claim 2~~ wherein the plurality of interconnects are formed on a plurality of levels, wherein nodes of Y's connecting clusters of a lower level are interconnected by Y's of a higher level.

4. (Original) The chip of claim 3 wherein each of the Y's on a particular level is oriented in a direction that is rotated by 90° from the Y's on a next lower level and is rotated by 90° from the Y's on a next higher level.

5. (Original) The chip of claim 1 wherein the chip has a shape of a convex polygon having at least five sides.

6. (Original) The chip of claim 5 wherein the polygon is symmetrical to directions of the interconnect.

7. (Original) The chip of claim 1 wherein each of the clusters comprises three cells arranged and routed in three symmetrical directions.

8. (Cancelled)

9-18. (Cancelled)

19. (Original) The chip of claim 4 wherein all cells are interconnected to other cells.

20-23. (Cancelled)

24. (Currently Amended) A chip comprising:

an array of hexagonal cells;

a plurality of interconnects including a plurality of Y's, each of the Y's respectively connecting the cells in clusters of three cells each, wherein the cells within the clusters are interconnected;

~~The chip of claim 1,~~ wherein each of the array of hexagonal cells includes a terminal for connecting to another cell;

wherein the Y connecting each cluster includes a node and three interconnects, each of the interconnects respectively connecting the node to a separate terminal in each of the three cells within the cluster;

wherein each Y connects each cell of its respective cluster of three cells to the node.

25. (Previously Presented) The chip of claim 1 wherein said array of hexagonal cells provides a hexagonal flow congestion pattern that does not include the center of the hexagonal pattern.

26. (Cancelled)

27. (Currently Amended) A chip comprising:

an array of hexagonal cells;

a plurality of interconnects including Y's connecting the cells in clusters of three adjacent cells each, wherein the cells in the clusters are interconnected;

~~The chip of claim 26~~ wherein the Y connecting each cluster has a node and three interconnects, each of the interconnects having an end connecting the node to a respective ~~ones~~ one of the cells within a cluster;

wherein each Y connects each cell of its respective cell group to the node.

28. (Currently Amended) A chip comprising:

an array of hexagonal cells;

a plurality of interconnects including Y's connecting the cells in clusters of three adjacent cells each, wherein the cells in the clusters are interconnected;

wherein the Y connecting each cluster has a node and three interconnects connecting the node to respective ones of the cells within a cluster;

wherein each Y connects each cell of its respective cell group to the node;

~~The chip of claim 27~~ wherein the plurality of interconnects are formed on a plurality of levels, wherein nodes of Y's connecting clusters of a lower level are interconnected by Y's of a higher level.

29. (Previously Presented) The chip of claim 28 wherein each of the Y's on a particular level is oriented in a direction that is rotated by 90° from the Y's on a next lower level and is rotated by 90° from the Y's on a next higher level.

30. (Cancelled)